| PTO-1449 REPRODUCED<br><br>**INFORMATION DISCLOSURE CITATION IN AN APPLICATION**<br><br>**July 15, 2003**<br><br>(Use several sheets if necessary) | ATTORNEY DOCKET NO.<br>0717.1063-007 | CONTINUATION OF APPLICATION<br>No. 09/465,140 | |
|---|---|---|---|
| | APPLICANT<br>Duy-Phach Vu, et al. | | |
| | FILING DATE | CONFIRMATION NO. | GROUP |

| OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)* | | |
|---|---|---|
| | AR | Akiyama, M., *et al.*, "Growth of GaAs on Si and Its Application to Fets and LEDs.", Nat. Res. Soc. Symp. Proc., 67:53-64 (1986). |
| | AS | Allen, *et al.*, "Characterization of Isolated Silicon Epitaxy Material", *SPIE*, Vol. 945 - Advanced Processing of Semiconductor Devices II (3/17-3/18, 1988). |
| | AT | Conference Record of the 1991 International Display Research Conference, October 15-17, 1991, *IEEE*. |
| | AU | Fan, *et al.*, "Lateral Epitaxy by Seeded Solidification for Growth of Crystal Si Films on Insulators", Appl. Phys. Lett., 38, 365, 3-1-81. |
| | AV | McClelland, *et al.*, "A Technique for Producing Epitaxial Films on Reusable Substrates", Appl. Phys. Lett., 37, 560, 9-15-80. |
| | AW | McDaniel, D.L., *et al.*, "Vertical Cavity Surface-Emitting Semi-Conductor Laser with CW Injection Laser Pumping", IEEE Photon Technol. Lett., March 23, 1990. |
| | AX | Milnes, A.G., "Semiconductor Heterojunction Topics: Introduction and Overview", Solid State Electronics, Vol. 29, 2:99-121 (1986). |
| | AY | Turner, G., *et al.*, "High-Speed Photoconductive Detectors Fabricated in Heteroepitaxial GaAs Layers", Mat. Res. Soc. Symp. Proc., 67:181188 (1986). |
| | AZ | Weber, J.P., *et al.*, "Effects of Layer Thickness Variations on Vertical Cavity Surface-Emitting DBR Semiconductor Lasers", IEEE Photon Tech. Ltr., March 23, 1990. |
| | AR2 | Yablonovitch, *et al.*, "Extreme Selectivity in the Lift-Off of Epitaxial GaAs Films", Appl. Phys. Lett., 51, 2222 12-28-87. |
| | AS2 | Sumiyoshi, *et al.*, Device Layer Transferred Poly Si TFT Array for High Resolution Liquid Crystal Projector", *IEEE*, 7.3.1-7.3.4, 1989. |
| | AT2 | Y. Hayashi, *et al.*, "A New Three Dimensional IC Fabrication Technology, Stacking This Film Dual-CMOS Layers", *IEEE IDEM*, pps. 657-660, 1991. |
| | AU2 | "3-D Chip on Chip Stacking", Semiconductor International, December 1991. |

| EXAMINER | 3/3/03 | DATE CONSIDERED | 7/3/03 |
|---|---|---|---|

| PTO-1449 REPRODUCED<br><br>**INFORMATION DISCLOSURE CITATION IN AN APPLICATION**<br><br>**July 15, 2003**<br><br>(Use several sheets if necessary) | ATTORNEY DOCKET NO.<br>0717.1063-007 | CONTINUATION OF APPLICATION<br>No. 09/465,140 | |
|---|---|---|---|
| | APPLICANT<br>Duy-Phach Vu, et al. | | |
| | FILING DATE | CONFIRMATION NO. | GROUP |

| OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)* | | |
|---|---|---|
| | AV2 | Matsumoto, *et al.*, "Liquid Crystal Displays (LCDs)", Electronic Display Devices, (John Wiley and Sons) pps. 29-84. |
| | AW2 | |
| | AX2 | |
| | AY2 | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

| EXAMINER | DATE CONSIDERED 3/3/05 |
|---|---|